WHAT IS CLAIMED IS:

1. A PLL circuit for use in a super-heterodyne receiver, comprising:

shifting means for shifting a predetermined frequency of a reference signal; and

control means for causing the shifting means to shift the predetermined frequency of the reference signal in a channel in which interference occurs.

2. The PLL circuit as set forth in Claim 1, further comprising:

a reference signal oscillating circuit for oscillating the reference signal, wherein the reference signal oscillating circuit includes an oscillating circuit, an oscillator, and an electrostatic capacitor for oscillating;

wherein the shifting means shifts an oscillating frequency of the reference signal frequency oscillating circuit by varying an electrostatic capacitance of the electrostatic capacitor for oscillating.

3. The PLL circuit as set forth in Claim 2, wherein:

the electrostatic capacitor is a variable capacitor.

4. The PLL circuit as set forth in Claim 1, further comprising:

a reference signal oscillating circuit for oscillating the reference signal, wherein the reference signal oscillating circuit includes (i) an oscillating circuit, (ii) an oscillator, (iii) a first electrostatic capacitor and a second electrostatic capacitor, which are for oscillating and are connected to each other in parallel, (iv) a switch for connecting and disconnecting the second electrostatic capacitor to and from the first electrostatic capacitor,

wherein:

the control means causes the switch to open or close, so as to shift the oscillating frequency of the reference signal oscillating circuit.

5. A television receiver comprising a PLL circuit for use in a super-heterodyne receiver,

wherein the PLL circuit includes (i) shifting means for shifting a predetermined frequency of a reference signal and (ii) control means for controlling the shifting means to shift the prescribed frequency of the reference signal in a channel in which interference occurs, and

wherein the television receiver uses a video IF frequency of 45.75 MHz, and a video RF frequency of 91.25 MHz in the channel in which interference occurs.

6. The television receiver as set forth in Claim 5,

further comprising:

a reference signal oscillating circuit for oscillating the reference signal, wherein the reference signal oscillating circuit includes an oscillating circuit, an oscillator, and an electrostatic capacitor for oscillating,

wherein the shifting means shifts the oscillating frequency of the reference signal frequency oscillating circuit by varying an electrostatic capacitance of the electrostatic capacitor for oscillating.

7. A beat reducing method for a television receiver, comprising the steps of:

shifting a reference signal frequency in a PLL circuit for a channel in which interference occurs; and

shifting a local oscillating frequency in accordance with the reference signal frequency so shifted, so as to shift an interfering spurious frequency of an intermediate frequency signal.

8. A PLL circuit for use in a super-heterodyne receiver, comprising:

a shifting circuit for shifting a predetermined frequency of a reference signal; and

a control circuit for causing the shifting circuit to shift the predetermined frequency of the reference signal

in a channel in which interference occurs.

9. A PLL circuit for use in a super-heterodyne receiver and for outputting a local oscillating signal, comprising:

a reference signal oscillating circuit for oscillating a reference signal used to determine a frequency of the local oscillating signal, wherein the reference signal oscillating circuit includes (i) an oscillating circuit, (ii) a shifting circuit for shifting a predetermined frequency of the reference signal oscillated by the oscillating circuit, (iii) a control circuit for causing the shifting circuit to shift the predetermined frequency of the reference signal in a channel in which interference occurs.